WHAT IS CLAIMED IS:

1. A programmable gain attenuator comprising:

a termination resistor;

a first termination switch connecting one side of the termination resistor to a first output;

a second termination switch connecting another side of the termination resistor to a second output;

a first resistor ladder arranged between a first input and the first side of the termination resistor;

a first plurality of switches each connecting a corresponding tap from the first resistor ladder to the first output, wherein the switches are connected in a first matrix;

a second resistor ladder arranged between a second input and the second side of the termination resistor; and

a second plurality of switches each connecting a corresponding tap from the second resistor ladder to the second output, wherein the switches are connected in a second matrix,

wherein some of the switches of the first plurality of switches are turned on for interpolation, and

wherein some of the switches of the second plurality of switches are turned on for interpolation.

2. The programmable gain attenuator of claim 1, wherein the first and second matrices each includes a fine matrix and a coarse matrix, which are controlled using fine and coarse selection logic, respectively, through a multiplexer.

3. The programmable gain attenuator of claim 1, wherein the switches in each of the first and second matrices are controlled so as to form corresponding submatrices with some of the switches in each submatrix on, and other switches off.

4. The programmable gain attenuator of claim 1, further including a plurality of resistors connected between the corresponding taps of the first and second resistor ladders.

5. A single-ended programmable gain attenuator comprising:

a termination resistor;

a termination switch connecting one side of the termination resistor to an output;

a resistor ladder arranged between an input and the one side of the termination resistor; and

a plurality of switches each connecting a corresponding tap from the resistor ladder to the output,

wherein the switches are connected in a matrix, and

wherein some of the switches of the first plurality of switches are turned on for interpolation.

6. The programmable gain attenuator of claim 5, wherein the matrix includes a fine matrix and a coarse matrix, which are controlled using fine and coarse selection logic, respectively, through a multiplexer.

7. The programmable gain attenuator of claim 5, wherein the switches are controlled so as to form a submatrix with some of the switches in the submatrix on, and other switches off.

8. The programmable gain attenuator of claim 5, further including a plurality of resistors connected between the corresponding taps of the first and second resistor ladders.

9. A single-ended programmable gain attenuator comprising:

a resistive ladder;

a plurality of switches corresponding to the resistive ladder and connected in a matrix to interpolate a desired voltage at the output, and connected to corresponding taps of the resistive ladders and to an output; and

a termination resistor.

10. A single-ended programmable gain attenuator comprising:

a resistive ladder;

a plurality of switches corresponding to the resistive ladder and connected to interpolate a desired voltage at the output, and connected to corresponding taps of the resistive ladders and to an output;

a termination resistor;

a fine selection logic for selection fine control switches out of the plurality of switches;

a coarse selection logic for selection fine control switches out of the plurality of switches; and

a multiplexer for passing control signals from the fine and coarse selection logic to the plurality of switches.

11. The programmable gain attenuator of claim 10, wherein the switches are arranged in a matrix.

12. A method of programming a gain of an attenuator comprising:

applying a differential input voltage to a first resistor ladder arranged between a first input and the first side of the termination resistor a termination resistor and to a second resistor ladder arranged between a second input and the second side of the termination resistor;

turning on some switches of a first plurality of switches arranged in a first matrix, while leaving other switches off, for interpolation of a desired voltage,

wherein the switches connect corresponding taps from the first resistor ladder to a first output;

simultaneously turning on some switches of a second plurality of switches arranged in a second matrix, while leaving other switches off, for interpolation of the desired voltage,

wherein the second plurality of switches connects corresponding taps from the second resistor ladder to a second output.